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10/623,028	07/17/2003	Derek Shaeffer	BBNT-T028	8766

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EXAMINER
CHERY, DADY

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,028	SHAEFFER ET AL.	
	Examiner	Art Unit	
	Dady Chery	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 is objected to because of the following informalities: It is not clear in the preamble of claim 14 if it is related to a method or a system. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 1, 3-6,8 –14,16,18-25 and 27 -30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song (US Patent 6,917,660, hereinafter Song) in the view of Lysdal et al. (US Patent 6,973,151, hereinafter Lysdal).

Regarding claim 1, Song discloses *a circuit* (Fig. 2A) *for multiplexing a plurality of data signals into an output data stream comprising:*

a plurality of circuit elements (24,23,27), *wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal* (Col. 2, lines 19 – 23), *wherein an output of each circuit element of said plurality of circuit elements comprises an individual data signal of said plurality of data signals*(Col. 4, lines 11 – 12 and Col. 2, lines 2 - 11) *and wherein said first clock signal is substantially in-phase with said transition* (Col. 3, lines 67 – Col. 4, lines 1);

a selector(22) *coupled to said plurality of circuit elements for sequentially selecting each of said individual data signals to generate said output data stream, wherein said selector is clocked to control said selecting by a second clock signal* (Col. 4, lines 10 – 35).

Song fails to *teach the second clock signal is out of phase with respect to the first clock signal by a fixed offset.*

However, Lysdal teaches a method where the second clock and first clock signal is out of phase by Δt (Col. 4, lines 4 –6). Which is the same function as described by the instant application.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the first and second signal out of phase in order to align the phase of the first clock signal and the phase of the second clock signal (Abstract).

Regarding claims 3,16, Song discloses *the method wherein said fixed offset comprises a delay* (Abstract).

Regarding claims 5, 18, song discloses *the method said delay is generated by a clock generator coupled to the selector* (Fig. 2A, 10 and abstract). Where the delay-locked loop (DLL) is considered as the clock generator.

Regarding claims 6, 19, Song discloses *the method wherein said clock generator comprises a coupled oscillator circuit* (Col. 3, lines 58 – Col. 4, lines 3). Where the counter is considered as the oscillator circuit.

Regarding claims 7, 20 and 27, Song discloses *the clock generator comprises a divide-by-two circuit* (Fig. 2a, A). The reference clock signal (REFCLK) has a divide-by-two circuit.

Regarding claims 8, 21, Song discloses *the method said delay comprises a propagation delay* (Abstract).

Regarding claims 9, 22 and 29, Song discloses *the circuit further comprising a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay* (Fig. 2A, Abstract and Col. 4, lines 10 –28).

Regarding claim 10, Song discloses *the circuit further comprising a compensator coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element, wherein said second clock signal is transmitted to said selector through said compensator* (Fig. 2A, Col. 5, lines 20 37).

Regarding claims 11 and 28, Song discloses *the circuit wherein said compensator retards said second clock signal to said selector by a compensating delay* (Col. 5, lines 25 – 31).

Regarding claim 12, Song discloses *wherein said compensating delay corresponds to said clock-to-data delay* (Col. 5, lines 20 – 23).

Regarding claims 13 and 30, Song discloses *the circuit wherein a part of said plurality of circuit elements comprises a flip-flop* (Col. 3, lines 39 –41). Where the latch with is the clock signal constitute a flip-flop.

Regarding claim 14, Song discloses *in a circuit* (Fig. 2A) *comprising a plurality of circuit elements* (24,23,27), *for providing a data signal with transitions in response to a clock signal and a selector* (22) *coupled to said plurality of circuit elements for selecting said data signal for an output data stream* (abstract), *a method for multiplexing a plurality of said data signals into an output data stream comprising*:

clocking said circuit elements with said first clock signal to control said transitions of said data signal (Col. 2, lines 19 – 23),

clocking said selector with said second clock to sequentially select a plurality of said data signals for said output data stream (Col. 4, lines 10 – 35).

Song fails to teach *providing first and second clock signals, wherein said second clock signal is out-of-phase with respect to said first clock signal by a fixed offset*.

However, Lysdal teaches a method where the second clock and first clock signal is out of phase by Δt (Col. 4, lines 4 –6). Which is the same function as described by the instant application.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the first and second signal out of phase in

order to align the phase of the first clock signal and the phase of the second clock signal (Abstract).

Regarding claim 23, Song discloses *the method further comprising the step of delaying said second clock signal by a compensating delay* (Abstract).

Regarding claim 24, Song discloses *the method wherein said compensating delay corresponds to a delay from said first clock signal to said transitions* (abstract).

Regarding claim 25, Song discloses as system for multiplexing (Fig. 2A) a plurality of data signals into an output data stream comprising:

a plurality of circuit elements (24,23,27), *wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal* (Col. 2, lines 19 – 23), *wherein an output of each circuit element of said plurality of circuit elements comprises an individual data signal of said plurality of data signals* (Col. 4, lines 11 – 12 and Col. 2, lines 2 - 11) *and wherein said first clock signal is substantially in-phase with said transition* (Col. 3, lines 67 – Col. 4, lines 1);

a selector(22) *coupled to said plurality of circuit elements for sequentially selecting each of said individual data signals to generate said output data stream, wherein said selector is clocked to control said selecting by a second clock signal* (Col. 4, lines 10 – 35).

a compensator coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element , wherein said second clock signal is transmitted to said selector through said compensator, wherein said compensator retards said second clock signal to said selector by a compensating delay corresponding to said clock-to-data delay (Abstract).

Song fails to *teach the second clock signal is out of phase with respect to the first clock signal by a fixed offset.*

However, Lysdal teaches a method where the second clock and first clock signal is out of phase by Δt (Col. 4, lines 4 –6). Which is the same function as described by the instant application.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the first and second signal out of phase in order to align the phase of the first clock signal and the phase of the second clock signal (Abstract).

5. Claims 2,4, 15,17 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Son in the view of Lysdal as applied to claims 1,14 and 25 above, and further in view of Kallman et al. (US Patent 5,774,508, hereinafter Kallman).

Regarding claims 2, 4, 15,17 and 26 Song in combination with Lysdal disclose the fixed offset, but they fail to mention the quadrature offset and delay.

However, Kallman teaches a method comprise a quadrature offset and delay (Col. 4, lines 54 – 63).

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a quadrature input in order to delay the quadrature portion of the signal so that subsequent sampling of latches will be measured at substantially equivalent times (Col. 4, lines 60 –63).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ozkan (US Patent 5,488,642) discloses a Digital Phase-Locked Loop Circuit.

Zwack (US Patent 5,052,028) discloses a Method for synchronizing the phase of clock signals of two clock generators in communication networks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dady Chery whose telephone number is 571-270-1207. The examiner can normally be reached on Monday - Thursday 8 am - 4 pm ESt.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dady Chery 08/13/2007

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER